REMARKS

Applicant respectfully requests reconsideration of the present U.S. patent application. The Specification was objected to because of an incorrect reference number. Claims 1 stands rejected under 35 U.S.C. § 102. Claims 2-17 stand rejected under 35 U.S.C. § 103. Claims 1, 7, 8 and 12 have been amended. Previously withdrawn claims 18-27 have been canceled. Claims 28-33 have been added. Therefore, claims 1-17 and 28-33 are pending.

Specification Objections

The Specification was objected to because of an incorrect reference number. Applicant has made an appropriate amendment to correct the reference number.

Claim Objections

Claim 8 was objected to because of the word "substrate." Applicant has amended claim 8 in such a way that there is no reference to "substrate." Applicant therefore respectfully submits that the claim objection has been overcome.

Claim Rejections - 35 U.S.C. § 102

Rejection of Claim 1 based on *Plumton*

Claim 1 was rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 5,243,207 issued to Plumton et al. (*Plumton*). For at least the reasons set forth below, Applicant submits that claim 1 is not anticipated by *Plumton*.

Claim 1 recites the following:

wherein the multi-layer structure includes a semiconductor substrate overlaid with a plurality of epitaxial semiconductor layers common to the D-mode and E-mode FETs, including a channel layer overlaid by a single barrier layer overlaid by a single etch stop layer overlaid by a first layer, ...

Claims 12 and 28 recite similar limitations.

Plumton discloses a merged BiFET process for fabricating heterojunction bipolar transistors (HBTs) integrated with heterojunction field effect transistors (HFETs). See Abstract; col. 3, lines 17-23. The process includes growing a cap layer over an emitter/gate layer, which is over FET enhancement channel and depletion channel layers, which is over a FET buffer layer, which is over a subcollector layer. See col. 3, line 26 – col. 4, line 10; Fig. 1e and Fig. 3. *Plumton* does not disclose a single barrier layer overlaid by a single etch stop layer overlaid by a first layer. Thus, *Plumton* fails to disclose at least one limitation of claims 1, 12 and 28. Consequently, claim 1 is not anticipated by *Plumton*. Applicant therefore respectfully requests that the Examiner withdraw the rejection of claim 1 under 35 U.S.C. § 102.

Claim Rejections - 35 U.S.C. § 103

Rejections of Claims 2-6, 12 and 15-17 based on *Plumton* in view of *Lai*

Claims 2-6, 12 and 15-17 were rejected under 35 U.S.C. § 103 as being unpatentable over *Plumton* in view of U.S. Patent No. 6,452,221 issued to Lai et al. (*Lai*). For at least the reasons set forth below, Applicant submits that claims 2-6, 12 and 15-17 are not rendered obvious by *Plumton* in view of *Lai*.

As explained above, *Plumton* does not disclose a single barrier layer overlaid by a single etch stop layer overlaid by a first layer, as recited in claims 1 and 12. Applicant agrees with the Examiner that *Plumton* fails to disclose all of the limitations of claims 2-6, 12 and 15-17. See Office Action, pages 4-8. However, Examiner contends that *Plumton* in view of *Lai* discloses the limitations of claims 2-6, 12 and 15-17.

Lai discloses an enhancement mode FET device that provides a Schottky barrier to inhibit undesirable surface depletion effects. See col. 1, lines 55-68. Applicant does not

necessarily agree with Examiner's interpretation of *Lai* as set forth in the Office Action and may choose to address such interpretation in response to other office actions, if necessary. However, regardless of whether the Examiner's interpretation of *Lai* is correct, Examiner does not assert that *Lai* discloses a single barrier layer overlaid by a single etch stop layer overlaid by a first layer, as recited in claims 1 and 12.

Therefore, *Lai* fails to cure the deficiencies of *Plumton* pointed out by Applicant. Thus, *Plumton* in view of *Lai* fails to disclose at least one limitation of claims 1 and 12. Consequently, claims 1 and 12 are not rendered obvious by *Plumton* in view of *Lai* for at least the reasons set forth above. Applicant therefore respectfully requests that the Examiner withdraw the rejection of claim 12 under 35 U.S.C. § 103.

Claims 2-6 depend from claim 1. Claims 15-17 depend from claim 12. Because dependent claims include the limitations of the claims from which they depend, Applicant submits that claims 2-6 and 15-17 are not rendered obvious by *Plumton* in view of *Lai* for at least the reasons set forth above. Applicant therefore respectfully requests that the Examiner withdraw the rejections of claims 2-6 and 15-17 under 35 U.S.C. § 103.

Rejections of Claims 7-13 based on *Oikawa* in view of *Lai*

Claims 7-13 were rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,078,067 issued to Oikawa (*Oikawa*) in view of *Lai*. For at least the reasons set forth below, Applicant submits that claims 7-13 are not rendered obvious by *Oikawa* in view of *Lai*.

Claim 7 recites the following:

wherein the multi-layer structure includes a semiconductor substrate overlaid with a plurality of epitaxial semiconductor layers common to the D-mode and E-mode FETs, including a channel layer overlaid by a single barrier layer overlaid by a single etch stop layer overlaid by a first layer overlaid by a second layer adjacent to the first layer, ...

Claim 12 recites similar limitations.

Oikawa discloses E-type and D-type FETs formed by sequentially growing on a semiconductor substrate a channel layer, an electron supply layer, a third semiconductor layer, a second etching stopper layer, a second semiconductor layer, a first etching stopping layer, and a first semiconductor layer. See Abstract; col. 7, line 45 – col. 8, line 3. *Oikawa* does not disclose a single barrier layer overlaid by a single etch stop layer overlaid by a first layer. Thus, *Oikawa* fails to disclose at least one limitation of claims 7 and 12.

Examiner contends that *Oikawa* in view of *Lai* discloses the limitations of claims 7-13. Applicant does not necessarily agree with Examiner's interpretation of *Lai* as set forth in the Office Action and may choose to address such interpretation in response to other office actions, if necessary. However, regardless of whether the Examiner's interpretation of *Lai* is correct, Examiner does not assert that *Lai* discloses a single barrier layer overlaid by a single etch stop layer overlaid by a first layer, as recited in claims 7 and 12. Therefore, *Lai* fails to cure the deficiencies of *Oikawa* pointed out by Applicant. Thus, *Oikawa* in view of *Lai* fails to disclose at least one limitation of claims 7 and 12. Consequently, claims 7 and 12 are not rendered obvious by *Oikawa* in view of *Lai* for at least the above reasons. Applicant therefore respectfully requests that the Examiner withdraw the rejections of claims 7 and 12 under 35 U.S.C. § 103.

Claims 8-11 depend from claim 7. Claim 13 depends from claim 12. Because dependent claims include the limitations of the claims from which they depend, Applicant submits that claims 8-11 and 13 are not rendered obvious by *Oikawa* in view of *Lai* for at least the reasons set forth above. Applicant respectfully requests that the Examiner withdraw the rejections of claims 8-11 and 13 under 35 U.S.C. § 103.

CONCLUSION

For at least the foregoing reasons, Applicant submits that the rejections have been overcome. Therefore, claims 1-17 and 28-33 are in condition for allowance and such action is respectfully solicited. The Examiner is respectfully requested to contact the undersigned by telephone if such contact would further the examination of the application.

Respectfully submitted,

Dated: December 11, 2006

Joseph A. Pugh
Reg. No. 52,137

TriQuint Semiconductor, Inc.
2300 NE Brookwood Parkway
Hillsboro, OR 97124
(503) 615-9616